



Job Profile	Job description	Offer
Digital System Architect	<p>Master degree in Electronic Engineering – Computer Engineering. We're looking for a experienced and motivated SoC design architect, to be part of a team developing challenging embedded solutions. The team is spread in many locations world wide.</p> <p>Expert in ARM CORTEX MX processors Expert in RTL (both VHDL and VERILOG) Expert in JTAG and SWD protocol Expert in UPF simulations Expert in SoC IPs integration Expert in firmware development to check correct IP integration Knowledge of scripting language.</p>	<p>Regular, full time contract Level 5' super CCNL Metalmeccanico</p>
Mobile/IoT Software Developer	<p>Master degree in Computer Science – Computer Engineering. Digital Information Technology (DIT) organization.</p> <p>Skills requested:</p> <ul style="list-style-type: none"> positive attitude, strong analytical and problem solving - proactive mindset - excellent team spirit <p>Dynamic team environment developing new cloud-based applications for end-to-end IoT and Mobile solutions, You'll contribute to promote great software design and quality, bringing innovation to evolve our applications. You'll be responsible to write well designed, testable code.</p> <p>Programming languages and technologies:</p> <p>Responsive mobile and WEB App development</p> <ul style="list-style-type: none"> - HTML5 / CSS3 / JavaScript - JQuery / JQuery Mobile, Bootstrap, SASS/LESS, NodeJS, ViuJS, Framework7, Ionic, WebPack - native application development on iOS and/or Android, Microsoft Xamarin / AppAccelerator - Define and/or refine UI and UX requirements <p>Added value:</p> <ul style="list-style-type: none"> - programming languages: Java, PHP, Python, C#, - Micro-Services Architecture (SOAP, REST) - Continuous Integration/Continuous Delivery, Maven, Jenkins, Cloud Native - Automated testing (server/client side) Test Driven Development, Junit, Mock Framework, Selenium, Jasmine - test practice on multiple device, using AWS Device Farm – Test Mobile Apps on Real Devices 	<p>Regular, full time contract Level 5' super CCNL Metalmeccanico</p>



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HW Designer	<p>Master degree in Electronic Engineering.</p> <p>The required position is within a design team developing RF and millimeter-wave ICs in BiCMOS and CMOS advanced processes. These devices target the automotive domain and in particular Radar, GNSS and Tuners applications.</p> <p>The candidate must be able to define the architecture of digital subsystems of the RFICs according to the device specification and customer requirements. In particular, he is required to write the RTL code of digital blocks that implement complex functions or are aimed to control the analog part of the chip.</p> <p>Moreover, where requested, he will be in charge of cross-domain check, logic synthesis, static timing analysis, DFT strategy and back annotated timing closure. Some digital back-end and mixed verification skills are desirable as well.</p> <p>The candidate should be experienced with coding languages like VHDL, Verilog and System Verilog and be able to work with different EDA tools like Simvision, Spyglass, Design compiler, Primetime and so on.</p>	<p>Regular, full time contract</p> <p>Level 5' super CCNL</p> <p>Metalmecanico</p>
Device Engineer	<p>Master degree in Physic.</p> <p>Gap analysis on VI-Power technology for Yield improvement. Failure analysis on wafers scrap (Parametric testing & EWS)</p> <p>Good attitude to work in Team and problem solving</p>	<p>Regular, full time contract</p> <p>Level 5' super CCNL</p> <p>Metalmecanico</p>
Digital Designer	<p>Master degree in Electronic Engineering – Computer Engineering.</p> <p>Assist in developing, writing, reviewing, and refining digital architecture specifications for custom digital ASICs. Participate in the development of next generation products. Interaction with Analog and ASIC RTL verification team, and support to backend team Specify, design, verify, and lab test hardware ASIC products.</p> <p>Deep understanding of all aspects of ASIC design flows and tools, Front End and Back End, RTL (Verilog/VHDL coding), Synthesis Flow, Static Timing analysis, DFT, CDC, linting, power optimizations technics, memGen. Floorplaning, PnR, IP integration, GDSII Experience with other related EDA tools such as Spyglass, linting, power estimator and CDC checking.</p> <p>Experience with implementing complex algorithms in hardware. Experience with Linux scripting languages. Hands on experience in designing digital circuits, writing complex test-cases in Verilog and/or System Verilog, and familiarity with code quality metrics.</p>	<p>Regular, full time contract</p> <p>Level 5' super CCNL</p> <p>Metalmecanico</p>

The Employment searches are addressed to candidates of both genders, under Law 10.04.1991 n. 125, as amended by Legislative Decree n. 198/2006 which guarantees gender equality at work

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